Abstracts

High frequency performance of a fully depleted 0.25-/spl mu/m SOI CMOS technology

D.D. Rathman, J.A. Burns, C.L. Chen, R. Berger, A.M. Soares and R.H. Mathews. "High frequency performance of a fully depleted 0.25-/spl mu/m SOI CMOS technology." 1999 MTT-S International Microwave Symposium Digest 99.2 (1999 Vol. II [MWSYM]): 577-580 vol.2.

A fully depleted (FD) 0.25-/spl mu/m silicon-on-insulator (SOI) CMOS process technology has been developed and established at Lincoln Laboratory. Here we describe the FDSOI process technology, report the high frequency performance of 0.25-/spl mu/m n- and p-channel MOSFETs and digital and analog circuits, and predict the performance of the FDSOI technology scaled to 0.1-/spl mu/m gate lengths.

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